Universal PHY ™

UCIe

UCIe is a recent standard for Die to Die connectivity and has been widely sold as the "Standard" for all applications.

Currently there are **3 incompatible** versions of UCIe:

UCIe-S is the version defined for mass markets – it is optimized for standard packaging.

UCIe-S is limited as it does not support redundancy and limited to 110-micron minimum pitch. It is also difficult to support with older nodes and implement for low power low cost, high reliability applications.

UCIe-S is primarily optimized for higher data rate applications – HPC.

UCIe – A and UCIe-3D both support advanced packaging with support for redundancy and lower power.

BOW

BOW started out earlier and has lost market traction to UCIe.
YorChip supports a new version of **BOW.Flexi** suitable for IOT and low cost, low power applications.

	UCIe-S	Universal PHY™
Max Lanes	16 per module	Up to 80 +
Area 16 lanes	1.6mm2	0.16 mm2
IOT Support	NO	Yes 0.04mm2
Redundancy	NO	YES
Power	0.6pj/bit	0.1pj/bit
3D support	NO	Yes
Advanced Packaging	NO	Yes

Universal PHY ™

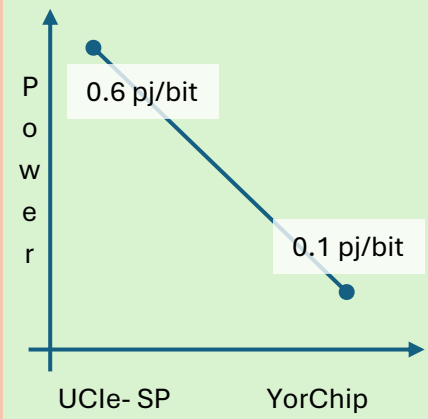
The core idea behind the Universal PHY™ is to enable open chiplets for a broad range of applications. **One** chiplet for a wide range of packaging and end applications.

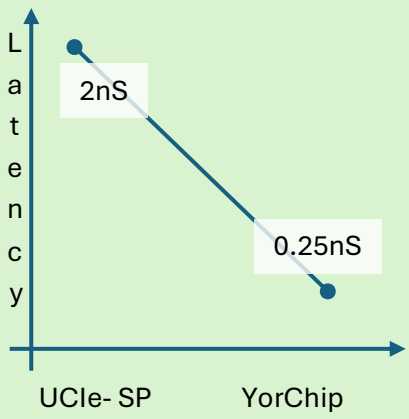
The PHY is protocol compliant with UCIe-S, UCIe-A and UCIe-3D. But uses unique bump map design and architecture.

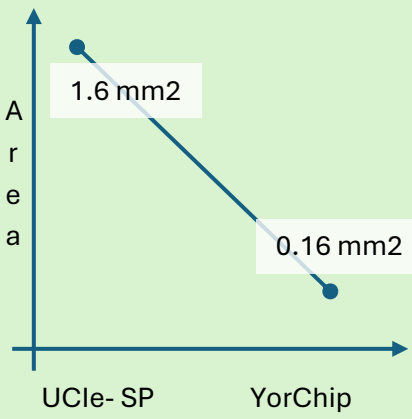
The Universal PHY ™ is patent-pending, and more details can be provided under NDA.

Unique Features:

Novel Redundancy for Hi-Rel, Support for 16&18-bit wide data, Support Synchronous Operation, Supports Advanced packaging, Support Control Data Signalling, Configurable no-clock option.







A much better PHY optimized for 40,28,22,16 nm and Size, Weight, Area, Power

Chiplet library in development : ADC, PCIe, Ethernet, Memory and FPGA
Package your ASIC chiplet with our library Chiplets to build your Full ASIC solution

Zero NRE PHY Cost to use Universal PHY™ in your next custom ASIC

Contact us for details : sales @ yorchip.com