Chiplet ASIC Flow

Open Chiplets?

Review with YorChip's design team status and availability of Open Chiplets within the ecosystem.

Save on IP costs, development and verification costs, if existing Open Chiplet can be used from our library.

Open Chiplets can also be modified and updated with shared costs if YorChip has interest for new features/versions within its ecosystem.

Open Chiplets in the works include:

FPGA – gives design flexibility in field.
ADC – suitable for high-speed signals and Software-Defined Radio (SDR) applications.
RISC-V suitable for AI at the edge with TPU and customization.
PCIe / Ethernet combo chiplet.
DDR/LPDDR memory support.
AI NPU optimized for edge AI.

Architecture

Floor planning the Chiplet ASIC is more complex as packaging is a critical part of the overall cost and performance architecture.

After reviewing Open Chiplets that can be used as-is – firm up the missing IP requirements.

If the Missing IP is a common interface YorChip may choose to share in IP cost/development.

Then ask for a formal quote on your ASIC Chiplet and for appropriate foundry process.

At this stage, an overall ASIC packaging floor plan needs to be planned that maximizes the use of the Open Chiplet with minimal area.

Joint design review to cover power, testability, thermal and packaging.

Time to Revenue

Getting product into the market first allows you to maximize profits.

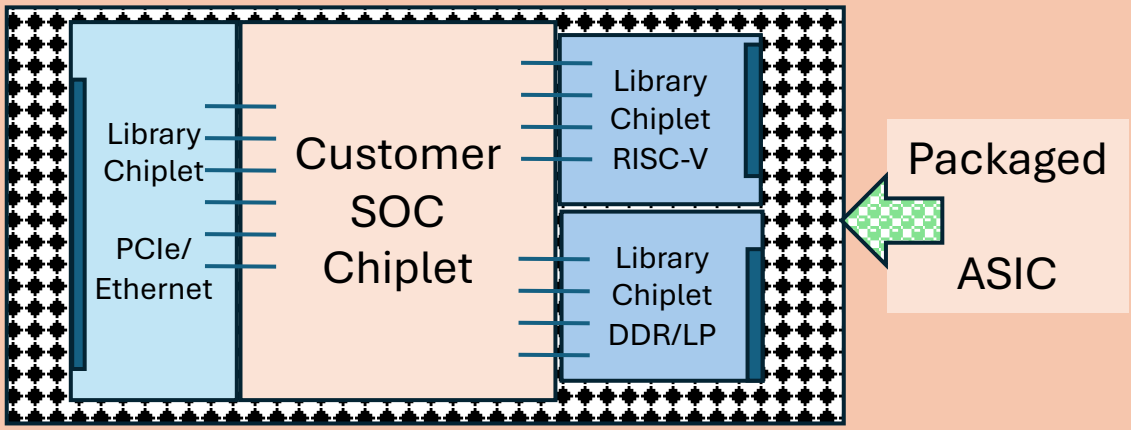
Chiplets enable new design flows as Open Chiplets focus overall risk to customers' own design.

The good news is on older nodes the foundries have prototyping runs almost monthly.

It may make sense to tape out early and start the packaging/test qualification process much earlier.

Even if the Chiplet ASIC needs a redo – the ability to get qualified and into production, generating revenue – cannot be overstated.

Incremental cost of a second prototype run, or if running risk production with a production mask set can be discussed with YorChip.



Chiplet library in development : ADC, PCIe, Ethernet, Memory and FPGA
Package your ASIC chiplet with our library Chiplets to build your Full ASIC solution

Zero NRE Cost to use our IP & Chiplets in your next ASIC

Contact us for details : sales @ yorchip.com