Chiplet-based ASIC

Today's ASIC options

A full-custom ASIC today is a great option for designers, as IP is readily available from many EDA vendors, Foundries and other companies.

Today's design tools coupled with Foundry PDKs lower the overall risk of failure.

Designers have many different foundries and process nodes to choose from.

With this plethora of solutions, however, there is a major problem.

Development costs of ASIC starts is exploding – due to ever increasing costs of IP, Masks, EDA Tools and increasingly shorter development windows in which to deliver.

And in today's AI-centric world, when algorithms are evolving rapidly, ASIC lead-times are pushed to limit.

FPGA to Rescue?

Traditionally, FPGAs have been a great way for designers to develop systems quickly at minimal cost.

This approach has worked well, and FPGAs are deployed in many systems ranging from data centers to automobiles.

While FPGAs deliver a broad range of logic density, they suffer from two major limitations.

Large FPGA performance & power have stopped scaling in accordance with Moore's Law.

Secondly, the FPGA architecture is not suitable for low-power, low-cost, high-performance applications due to excessive size, weight, cost and power limits.

As edge devices get smarter – large system FPGA may not be viable.

Chiplets to Rescue!

There has been enormous hype on the Chiplet revolution, but it has not resulted in widespread adoption for Mass Markets.

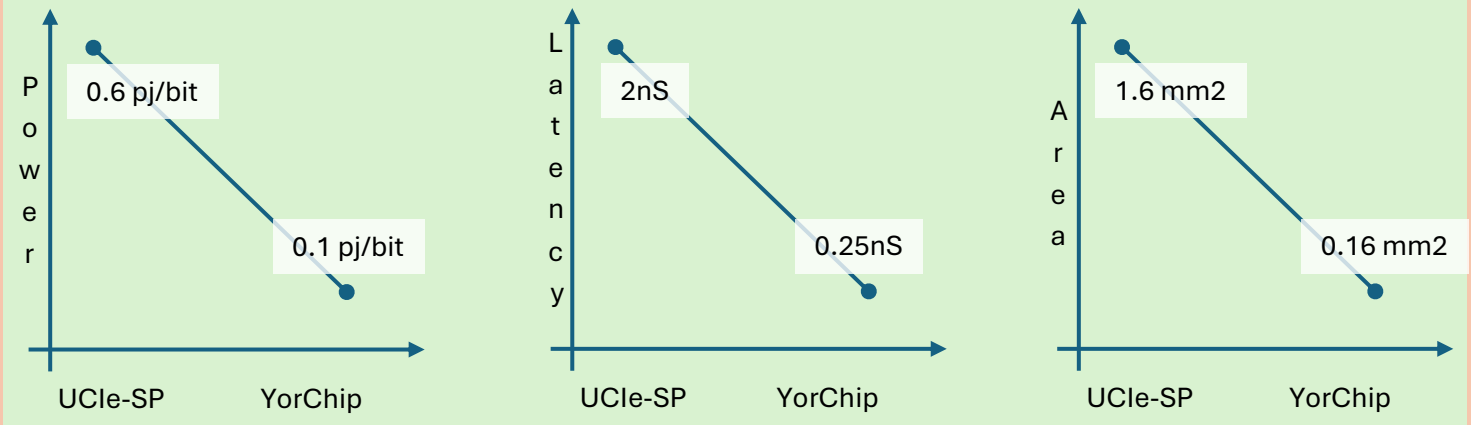
The reality is that the IP standards, like UCIe, and major EDA vendors have focused on HPC and Data Center markets.

IP is currently priced in Millions of Dollars and is not even available at common nodes like 40, 28, 22, 16nm etc.

Unfortunately, the standards bodies have not optimized their IP for lower cost, lower area, and lower latency.

YorChip is developing chiplets for use in customer SOCs using its patent-pending Universal PHY™.

Consider a Chiplet-based ASIC.



A much better PHY optimized for 40,28,22,16nm and Size, Weight, Area, Power

Chiplet library in development : ADC, PCIe, Ethernet, Memory and FPGA

Package your ASIC chiplet with our library Chiplets to build your Full-ASIC solution

Zero NRE Cost to use our IP & Chiplets in your next ASIC

Contact us for details : sales @ yorchip.com