100G Ultra MAC/PCS designed by SiliconIPs

Ethernet MAC & PCS

100G Ethernet MAC and PCS have been stable and adopted in the market for many years and used extensively in ethernet transport for home, industrial and data center markets.

Recent requirements driven by AI training and inference driving more stringent latency and link management are now being developed.

Ultra Ethernet is a new upcoming standard being adopted to improve AI support to reduce tail latency and improve overall system level performance, congestion and overall management.

To find out more on Ultra Ethernet visit: https://ultraethernet.org/

The Ultra MAC can be licensed with Ultra Ethernet Support.

Low Power& latency

Generally, solutions in the market are not optimized for lower latency or low gate count (hence lower power).

The Ultra MAC is architected for lowest latency and size/power.

It is designed to support both 25G NRZ PAM 2 PHY as well as 106G PAM 4 PHY and multiple FEC options.

Key advantage of NRZ PHY is it is possible use without FEC, making it ideal for clustering CPU & edge AI applications.

For lowest latency – the recovered clock is used for MAC/PCS operation for both versions.

Todays AI and edge applications require lowest latency & power.

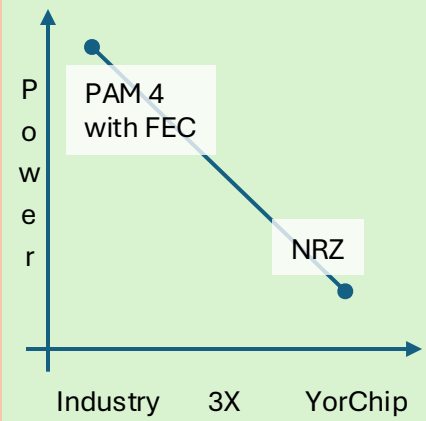
Ultra Ethernet

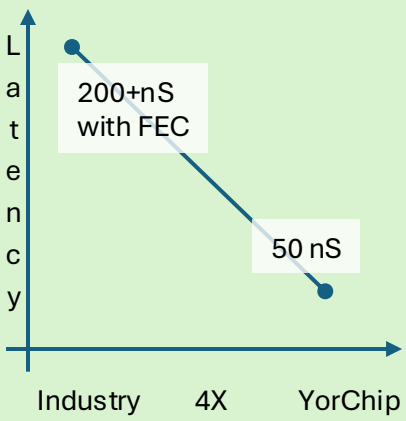
This IP supports insertion and deriving Control Ordered Set (CtlOS). The Control Ordered Set (CtlOS) is a message mechanism utilized by the UEC Link Layer which features Credit-Based Flow Control (CBFC) and Link-Level Retry (LLR).

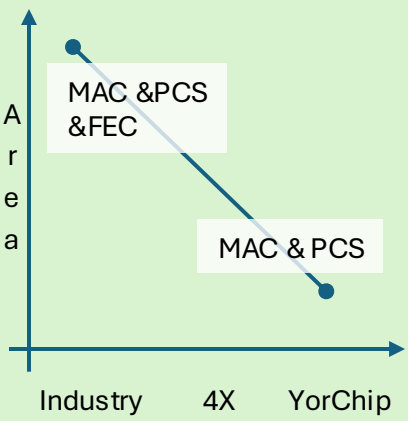
This IP generates CtlOS on transmit side based on the data provided by the application over a dedicated interface.

On the receive side the IP derives the CtlOS from the incoming traffic and delivers the payload data to the application over the dedicated interface.

This IP is designed to work with upper link layers to enable designers to build a low power low latency Ultra Ethernet link.







Ultra MAC and PCS optimized for AI and Edge devices

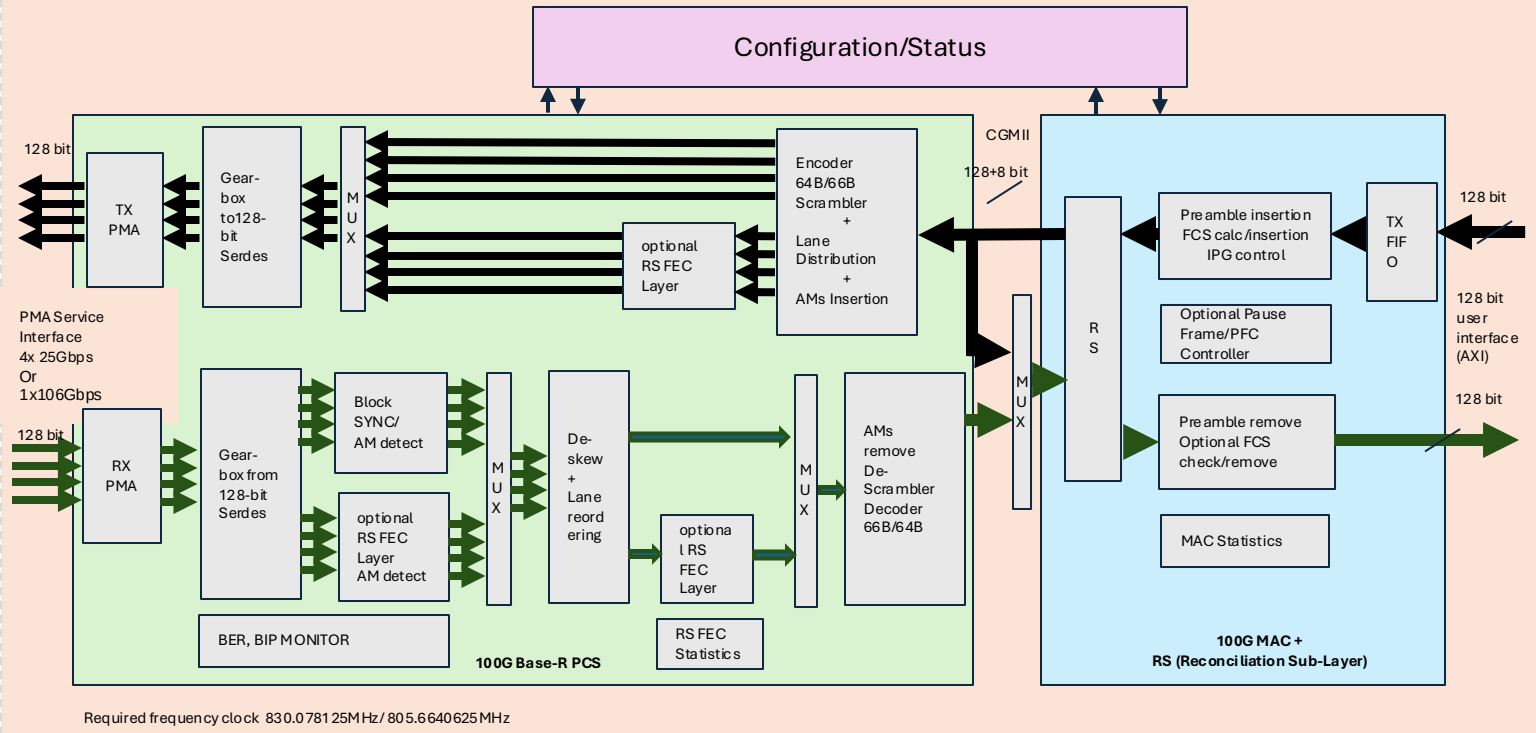
YorChip can provide IP or provide Chiplets with Ultra MAC/PCS with NRZ PHY or PAM 4 for Sale

This PHY is designed by SIliconIPs and sold by YorChip

Contact us for details : sales @ yorchip.com

100G Ultra MAC/PCS designed by SiliconIPs

Ultra Low Latency MAC/PCS Architecture



Required frequency clock 830.078125MHz/ 805.6640625MHz

The IP integrates MAC Layer, RS Sub-Layer and 100G PCS Base-R cores according to IEEE 802.3 standard to provide seamless connection between an application and serdes interfaces

128-bit interface for TX and RX between MAC and the application

Serdes interface – configurable to support PAM2 and PAM 4:

a. 4x lanes of 32 bits (25G NRZ)
b. 2x lanes of 64 bits(2-to-1bit muxing) (2x53G PAM 4)
c. 1x lanes of 128 bits (4-to-1 bit muxing)(1x106G PAM 4)

The MAC optionally supports FCS (CRC-32) calculation and insertion (TX) and check and striping (RX)

IPG: three modes:

- Minimum 12 bytes (Standard, default)
- Average 12 using the deficit idle count (DIC) (Standard)
- Minimum possible (back-to-back packets) – depending on the packet sizes, the IPG is between 1 and 8 bytes.

Optional support for User defined preamble

Optional support for Pause Frame/Priority Frame Control PFC handling

Optional support for Reed-Solomon Forward Error Correction (RS-FEC) including RS(528,514) and RS(544,514) for 100G-KR and 100G-KP. Lower Latency RS-FEC – (272,257)

Operational clock frequency: 805.6640625 MHz (IEEE 802.3 Clause 82 with no RS FEC or IEEE 802.3 Clause 82 with Clause 91 for RS FEC (528,514))830.078125MHz (IEEE 802.3 Clause 82 with Clause 91 for RS FEC (544,514)) or with RS FEC (272,257)

Latency (numbers are given for synchronous design as shown on the block diagram):

No RS FEC enabled:

TX ~25 ns.
RX ~31 ns.

With RS FEC enabled:

TX ~27 ns. (estimations)
RX ~130 ns. (estimations based on RS FEC partner numbers for the Decoder) (544,514)
RX ~105 ns. (estimations based on RS FEC vendor numbers for the Decoder) (528,514)
RX ~80 ns. (estimations) (272,257)
RX ~230 ns (estimations, Interleaved RS FEC according to 802.3ck RS(544, 514)

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